(A) generating an enumeration of a plurality of fuses in said design;

(B) compiling data for each of said fuses, wherein said data comprises simulation path data; and

(C) simulating said design with at least one of said fuses programmed for said repair to verify said repair.

2. (AMENDED) The method according to claim 1, wherein said simulation path data comprises verilog simulation path data.

3. (AMENDED) The method according to claim 14, wherein said schematic path data comprises at least one of a schematic path, a property, a hierarchy and a verilog path.

4. (TWICE AMENDED) The method according to claim 1, wherein step (B) further comprises the sub-step of:

generating a list of layout coordinates and paths in said design as part of said compiling.

5. (AMENDED) The method according to claim 1, further comprising the step of:

generating a fuse report.

6. (AMENDED) The method according to claim 5, further comprising the step of:

listing physical locations of a device in said design in response to said fuse report.

7. (AMENDED) The method according to claim 1, further comprising the step of:

generating a repair file that predicts said at least one of said fuses programmed for said repair.

8. (AMENDED) The method according to claim 7, further comprising the step of:

creating a repair program in response to said repair file.

9. (AMENDED) The method according to claim 8, further comprising the step of:

verifying a function of said design in response to said repair program.

10. (AMENDED) The method according to claim 8, further comprising the step of:

listing an output of said repair program as a list of coordinates for said at least one of said fuses programmed for said repair in terms of a plurality of logical addresses.

11. The method according to claim 10, further comprising the step of:

storing said coordinates in a memory.

12. (AMENDED) An apparatus comprising:

a first circuit configured to enumerate a plurality of fuses in a design; and

a second circuit configured to (i) compile data for each of said fuses, wherein said data comprises simulation path data and (ii) perform a simulation said design with at least one of said fuses programmed for a repair of said design to verify said repair.

13. (AMENDED) An apparatus comprising:

means for generating an enumeration of a plurality of fuses in a design;

means for compiling data for each of said fuses, wherein said data comprises simulation path data; and

means for simulating said design with at least one of said fuses programmed for a repair of said design to verify said repair.

14. The method according to claim 1, wherein said data further comprises schematic path data.

15. The method according to claim 1, wherein said data further comprises physical location data.

16. The method according to claim 1, further comprising the step of:

mapping a plurality of co-ordinates of said fuses to a plurality of verilog program statements.

17. The method according to claim 8, further comprising the step of:

checking said repair file and said repair program for an error.

18. The apparatus according to claim 12, wherein said first circuit is further configured to provide an elevation of said fuses at least one level of abstraction in said design.

19. The apparatus according to claim 12, wherein said first circuit is further configured to collect data relevant to said fuses that are grouped.

20. The apparatus according to claim 12, wherein said second circuit is further configured to write a report file.